**Verilog Code for Full Adder Data Flow Model**

module fadder(

input A,B,C,

output S,CO

);

assign S = A ^ B^ C;

assign CO = (A&B) + (A&C) + (B&C);

endmodule

**Verilog Code for Half Adder Behavioral Model**

module fadder(

input wire A,B,C,

output reg S,CO

);

always @ (A or B)

begin

if (A==0&&B==0&&C==0)

begin

S = 0;

CO = 0;

end

if (A==1&&B==0&&C==0)

begin

S = 1;

CO = 0;

end

if (A==0&&B==1&&C==0)

begin

S = 1;

CO = 0;

end

if (A==0&&B==0&&C==1)

begin

S = 1;

CO = 0;

end

if (A==1&&B==1&&C==0)

begin

S = 0;

CO = 1;

end

if (A==1&&B==0&&C==1)

begin

S = 0;

CO = 1;

end

if (A==0&&B==1&&C==1)

begin

S = 0;

CO = 1;

end

if (A==1&&B==1&&C==1)

begin

S = 1;

CO = 1;

end

end

endmodule

**Verilog Code for Full Adder Structural Model**

module fadder(

input A,B,C,

output S,CO,

inout x1,x2,x3

);

xor xor1(S,A,B,C);

and and1(x1,A,B);

and and2(x2,B,C);

and and3(x3,A,C);

or or1(CO,x1,x2,x3);

endmodule